2-Phase Unipolar Stepper Motor Driver

SLA707xM Series

February, 2006

■General Description

Combining low-power CMOS logic with high-current, high-voltage power FET outputs, the Series SLA707xM translator/drivers provide complete control and drive for a two-phase unipolar stepper motor with internal fixed off time and pulse-width modulation (PWM) control of the output current in a power multi-chip module (PMCM™).

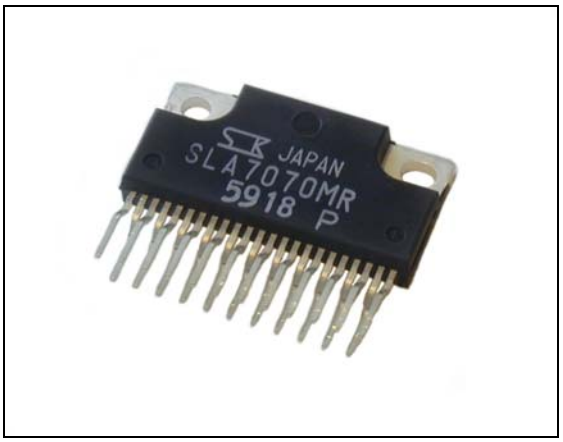
There are no phase-sequence tables, high-frequency control lines, or complex interfaces to program. The CMOS logic section provides the sequencing logic, direction, control, synchronous/asynchronous PWM operation, and a "sleep" function. The minimum CLOCK input is an ideal fit for applications where a complex µP is unavailable or overburdened. TTL or LSTTL may require the use of appropriate pull-up resistors to ensure a proper input-logic high. For PWM current control, the maximum output current is determined by the user's selection of a reference voltage and sensing resistor. The NMOS outputs are capable of sinking up to 1, 1.5, 2, or 3 A (depending on device) and withstanding 46 V in the off state.

Clamp diodes provide protection against inductive transients. Special power-up sequencing is not required.

Full-,and Half-step operation are externally selectable for the SLA7070/71/72/73MR. Full-, Half-, quarter-, and eighth-, and sixteenth-step operation are externally selectable for the SLA7075/76/77/78MR.

Half-step excitation alternates between the one-phase and two-phase modes (A-AB-B-AB-A-AB-BAB),providing an eight-step sequence.

■Package—SLA23Pin



■Applications

- PPC
- Printer
- OA Equipment

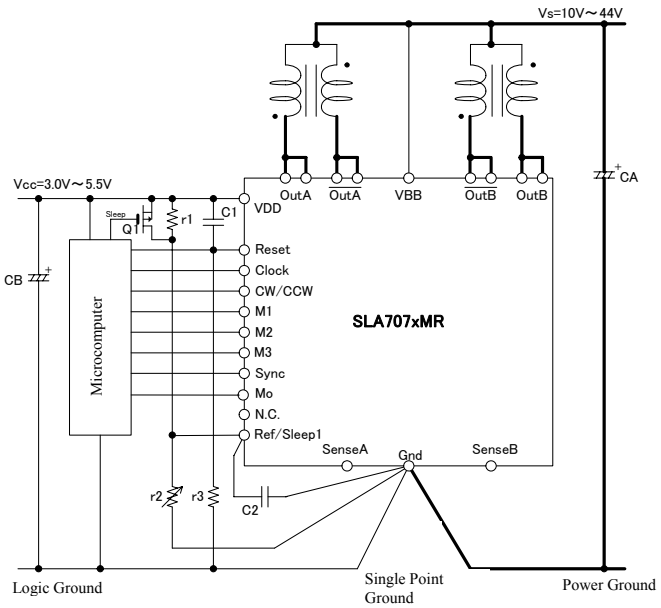
■Features

- To 3 A Output Rating
- Internal Sequencer for Microstepping Operation
- PWM Constant-Current Motor Drive
- Cost-Effective, Multi-Chip Solution
- 100 V, Avalanche-Rated NMOS Outputs
- Low RDS(on) NMOS Outputs (150 milliohms typical)
- Advanced, Improved Body Diodes
- Inputs Compatible with 3.3 V or 5 V Control Signals
- Sleep Mode
- Internal Clamp Diodes

■Key Specifications

- Motor Supply Voltage (VM): 44V max
- Load Supply Voltage (Vs): 10V to 44V
- Logic Supply Voltage (Vcc): 3V to 5.5V
- Output Current (Io): 1A(SLA7070MxRxx, SLA7075MxRxx)
  1.5A(SLA7071MxRxx, SLA7076MxRxx)
  2A(SLA7072MxRxx, SLA7077MxRxx)
  3A(SLA7073MxRxx, SLA7078MxRxx)
  The x represents P, W, or R according to the functions (See App Note).
- Output Maximum Voltage (V_{DSS}): 100V min

Typical Connection



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Scope

The present specifications shall apply to a micro-stepping capable 2-phase unipolar stepper motor driver IC, SLA7077MR and shall apply to the devices compliant with RoHS Directive.
Lead part solder: Pb free. Inner solder: Containing Pb > 85%.
* Please refer to the electric characteristics in the application note for other devices of the series.

Outline

Type	Hybrid integrated circuit
Structure	Plastic molded (transfer mold)
Applications	To drive a 2-phase stepper motor. (Micro-Stepping Capable. PWM Constant-Current Control.)

Absolute maximum ratings

Parameter	Symbol	Ratings	Unit	Remarks
Load Supply Voltage	V_M	46	V	
Main Power Supply Voltage	V_{BB}	46	V	
Logic Supply Voltage	V_{DD}	7	V	
Output Current	I_O	2.0*	A	Vref=0.4V, Mode F
Logic Input Voltage	V_{IN}	-0.3 to V_{DD}+0.3	V	
REF Input Voltage	V_{REF}	-0.3 to V_{DD}+0.3	V	
Sense Voltage	VRS	±2	V	Except for tw<1μs
Power Dissipation	PD	4.7	W	At Ta=25°C
		17	W	At Tc=25°C
Junction Temperature	Tj	150	°C	
Operating Temperature Range	Ta	-20 to 85	°C	
Storage Temperature Range	Tstg	-30 to 150	°C	

*Output current rating may be limited by duty cycle, ambient temperature, and heat sinking.
Under any conditions, do not exceed the specified junction temperature(T_j).

Electrical characteristics

Recommendable Operating Range

Parameter	Symbol	Ratings		Unit	Remarks
		MIN	MAX		
Load Supply Voltage	V_M		44	V	
Main Power Supply Voltage Range	V_{BB}	10	44	V	
Logic Supply Voltage Range	V_{DD}	3.0	5.5	V	Please adjust the Vcc surge voltage to 0.5V or less.
REF Input Voltage Range	V_{REF}	0.04	0.4	V	The control current accuracy decreases in 0.1V or less.
Case Temperature	T_C		90	°C	12Pin temperature (With no Fin)

Electrical Characteristic (T_a=25°C,V_{BB}=24V,V_{DD}=5V Unless Otherwise Noted.)

Parameter	Symbol	Limits			Unit	Test Condition
		Min.	Typ.	Max.		
Main Power Supply Current	I_{BB}			15	mA	Regularity
	I_{BBS}			100	μA	at SLEEP operation
Logic Supply Current	I_{DD}			5	mA	
Drain-Source Breakdown	$V_{(BR)DS}$	100			V	V_{BB}=44V I_D=1mA
Output On Resistance	$R_{DS(on)}$		0.25	0.4	Ω	Io=2A
Body Diode Forward Voltage	V_F		0.95	1.2	V	Io=2A
Maximum Clock Frequency	f_{clk}	250*			kHz	duty=50%
Logic Input Voltage	V_{LIL}			0.25 V_{DD}	V	
	V_{LIH}	0.75V_{DD}			V	
Logic Input Current	I_{LIL}		±1		μA	
	I_{LIH}		±1		μA	
REF Input Voltage Range	V_{REF}	0		0.45	V	Stationary current control
	V_{REFS}	2.0		V_{DD}	V	at SLEEP operation

*Operation at a step frequency greater than the specified minimum value is possible but not warranted.

Note.
Negative current is defined as the outflowing current from the specified pin.

REF Input Current	I_{REF}		±10		μA	V_{REF}=0 to V_{DD}
Logic Output Voltage	V_{LOL}			1.25	V	I_{LOL} =1.25mA
	V_{LOH}	V_{DD}-1.25			V	I_{LOH} =-1.25mA
Logic Output Current	I_{LOL}			1.25	mA	
	I_{LOH}	-1.25			mA	

Operation at a step frequency greater than the specified minimum value is possible but not warranted.

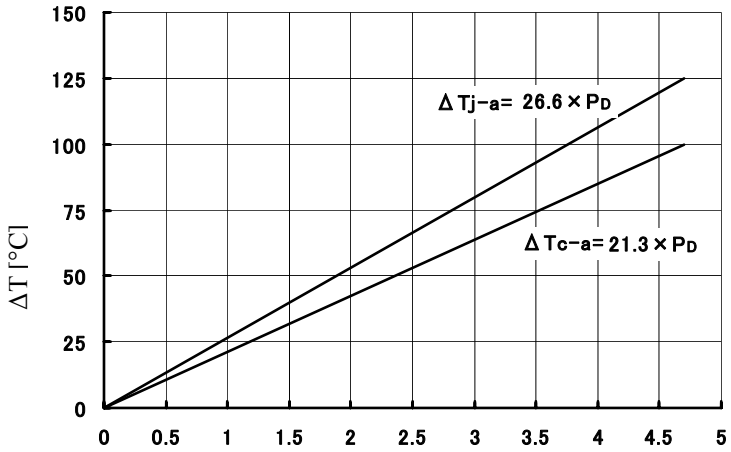
Note.
Negative current is defined as the outflowing current from the specified pin.

Electrical Characteristic(continued) (T_a=25°C,V_{BB} =24V,V_{DD} =5V Unless Otherwise Noted.)

Characteristic	Symbol	Limits			Unit	Test Condition
		Min.	Typ.	Max.		
Sense Voltage	V_{SENSE}		0.3		V	V_{REF}=0.3V Mode F
Current detection Resistance	Rs	0.199	0.205	0.211	Ω	
Step Reference Current Ratio	Mode F		100		%	V_{REF}=0.04V to 0.4V
	Mode E		98.1		%	
	Mode D		95.7		%	
	Mode C		92.4		%	
	Mode B		88.2		%	
	Mode A		83.1		%	
	Mode 9		77.3		%	
	Mode 8		70.7		%	
	Mode 7		63.4		%	
	Mode 6		55.5		%	
	Mode 5		47.1		%	
	Mode 4		38.2		%	
	Mode 3		29.0		%	
	Mode 2		19.5		%	
	Mode 1		9.8		%	
Wake-Up time	t_{SE}	100			μs	Sleep1 & Sleep2
Switching Time	t_{pdon}		2.0		μs	Clock→Out ON
	t_{pdoff}		1.5		μs	Clock→Out OFF
PWM Minimum On Time	$t_{ON(min)}$		1.7		μs	
PWM OFF Time	t_{OFF1}		12		μs	Mode 8 to F
	t_{OFF2}		9		μs	Mode 4 to 7
	t_{OFF3}		7		μs	Mode 1 to 3

Note.
・Negative current is defined as coming out of the specified pin.

Thermal Design Data



Truth Table

・Input Pin

Name	Low Level	High Level	Clock
Reset	Run	Logic Reset	-
CW/CCW	Forward (CW)	Reverse(CCW)	
M1 M2 M3	Micro-Stepping Operation Mode Setting		
Ref		Sleep Mode 1*	-
Sync	Asynchronous PWM Operation	Synchronous PWM Operation	-

* With a setup of a sleep mode 1, the operation is "Output Disable" and "Sequencer Enable"

Micro-Stepping Operation Mode Setting

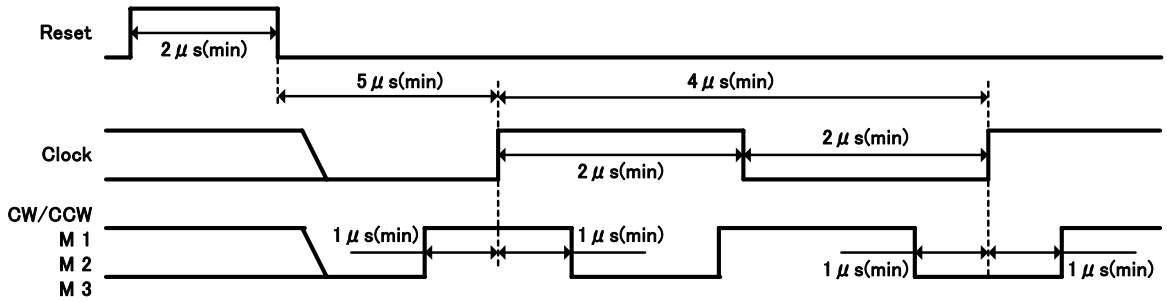
Operation Mode	M1	M2	M3	Remarks
2 Phase(1 Step)	L	L	L	Mode 8 only
2Phase(1 Step)	H	L	L	Mode F only
1-2 Phase(1/2 Step)	L	H	L	Mode 8, F
1-2 Phase(1/2 Step)	H	H	L	Mode F
W1-2 Phase(1/4 Step)	L	L	H	Mode 4,8,C,F
W1-2 Phase(1/8 Step)	H	L	H	Mode 2,4,6,8,A,C,E,F
4W1-2 Phase(1/16 Step)	L	H	H	Mode 1 to F
Sleep Mode 2*	H	H	H	

* With a setup of a sleep mode 2, the operation is "Output Disable" and "Sequencer Hold". Sleep mode 2 operates without depending on the Clock.

Output Pin

Pin Name	High Level	Low Level
Mo	Half-Step Position (Mode 8)	-

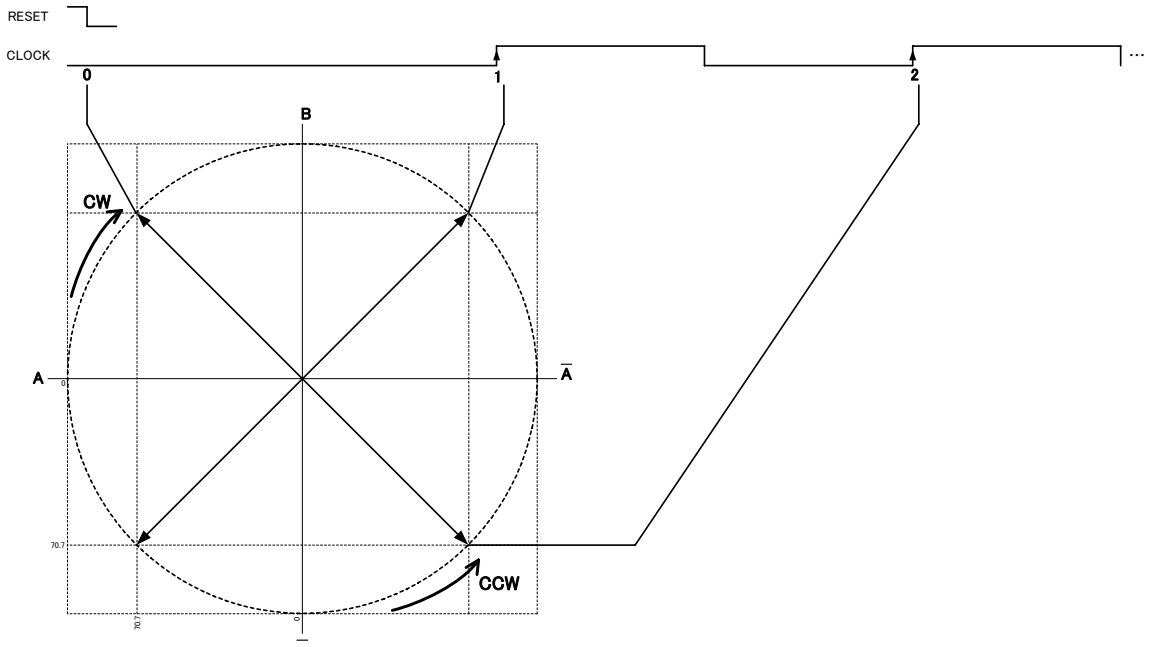
Logic Input Timing Requirements



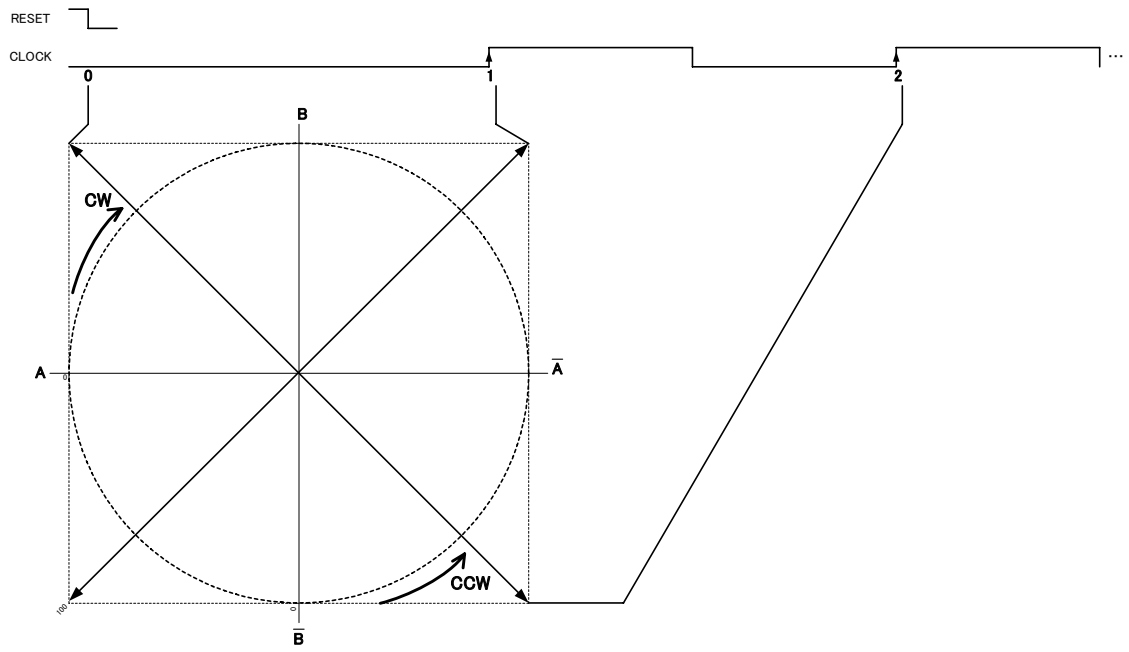
Step Sequencing Chart

2Phase

Mode: 8 M1: L, M2: L, M3: L

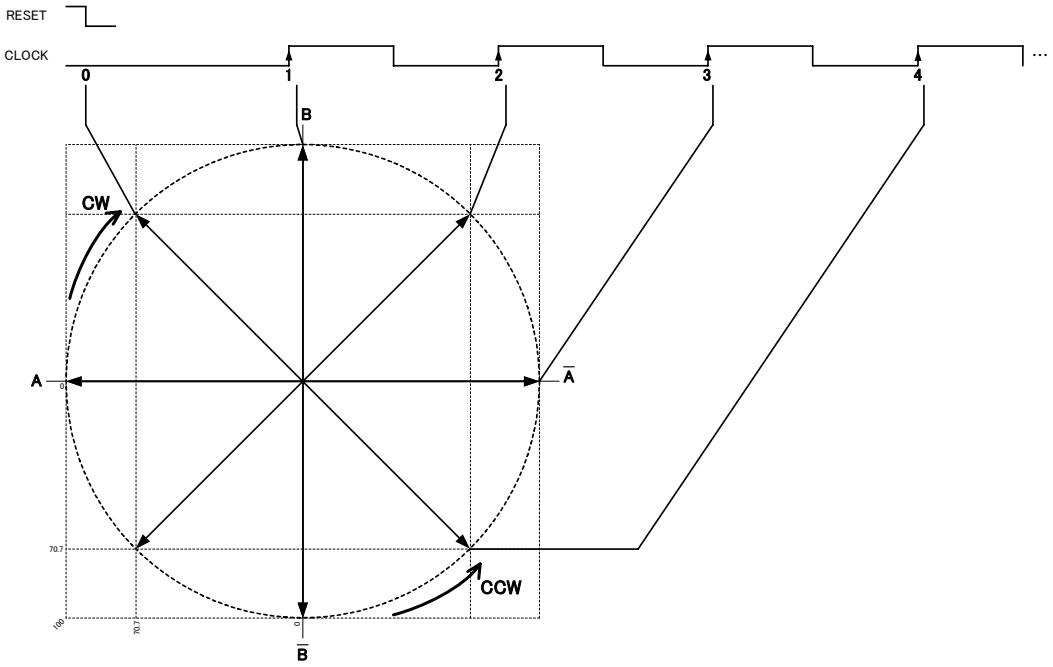


Mode: F M1: H, M2: L, M3: L

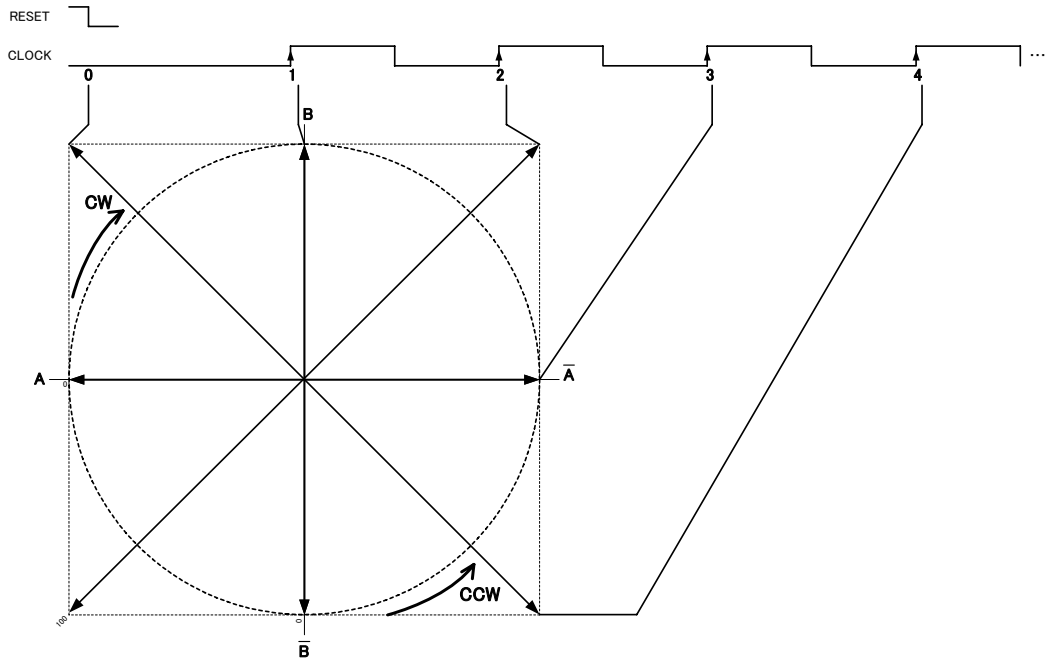


1-2Phase

Mode: 8 <=> F M1: L, M2: H, M3: L



Mode: F M1:H, M2: H, M3: L



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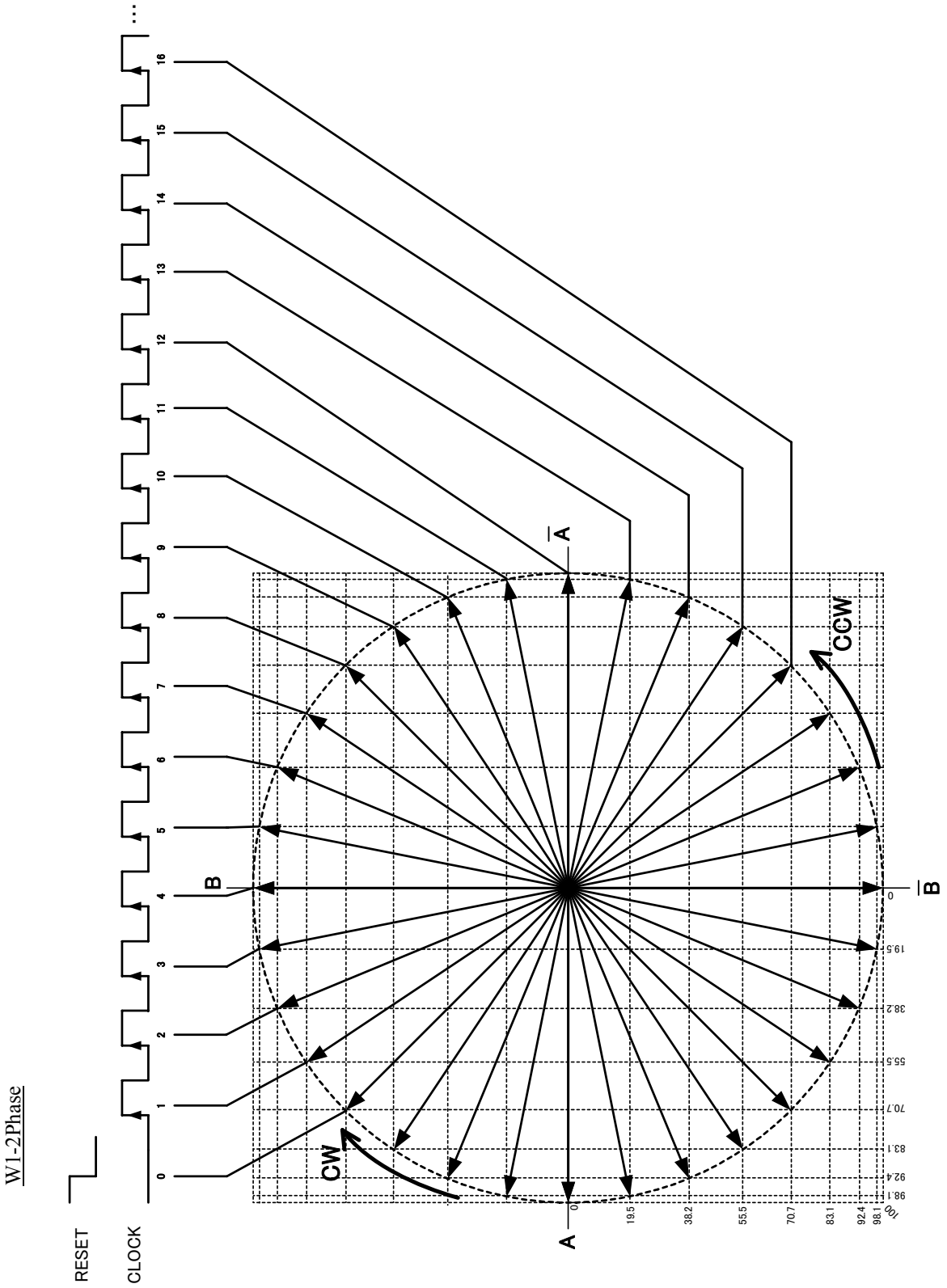

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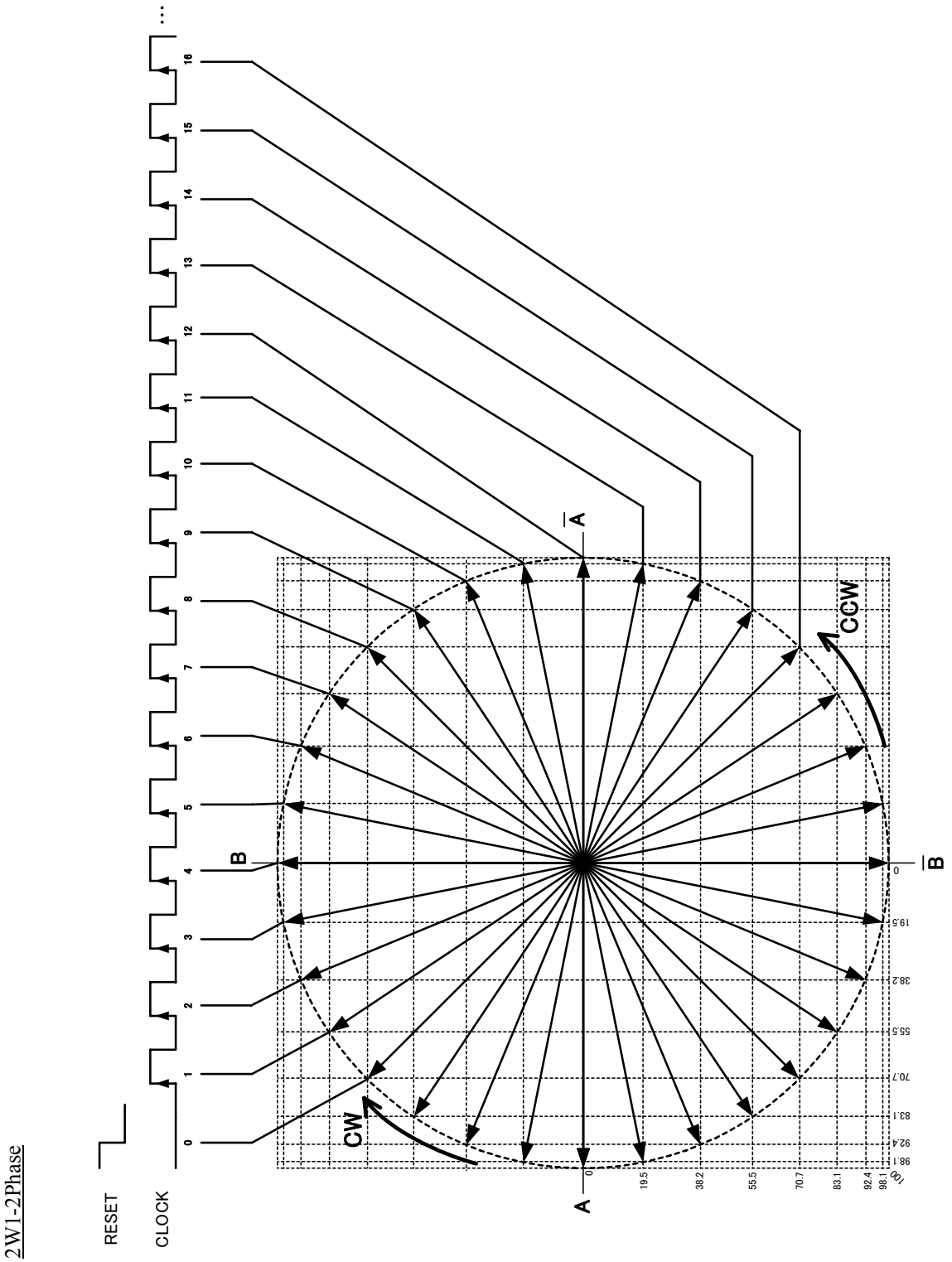
2W1-2Phase



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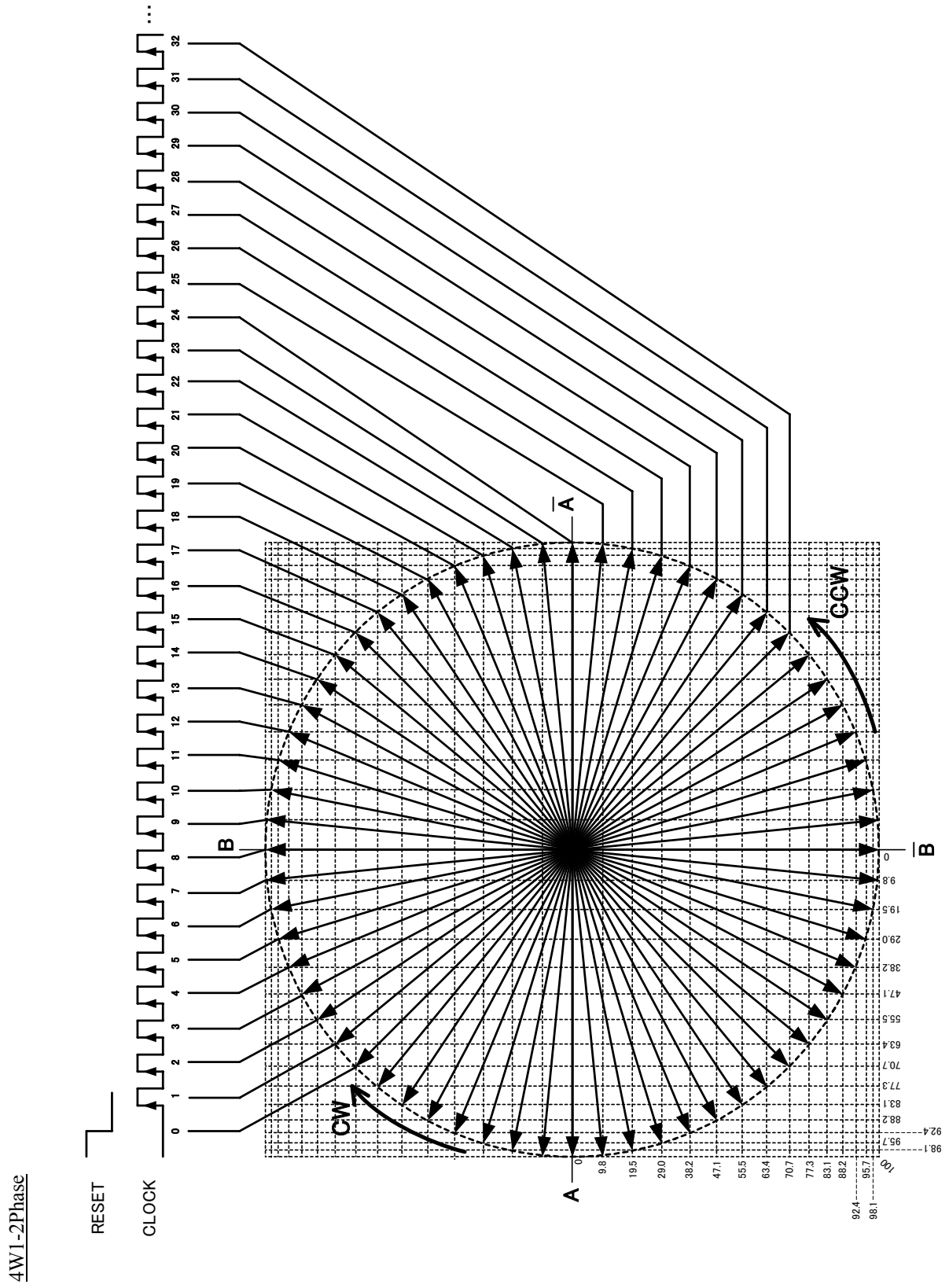

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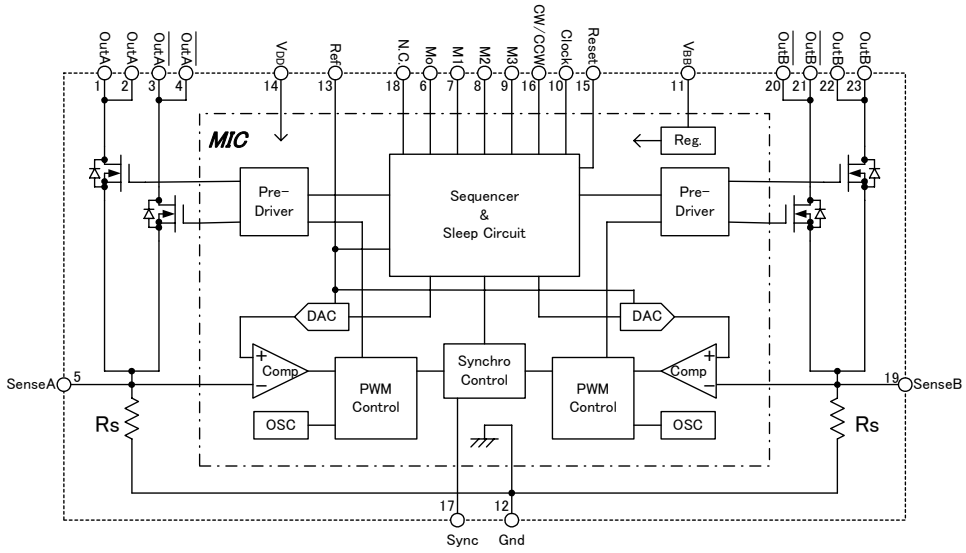
Block diagram (Connection diagram)

Internal functional block diagram

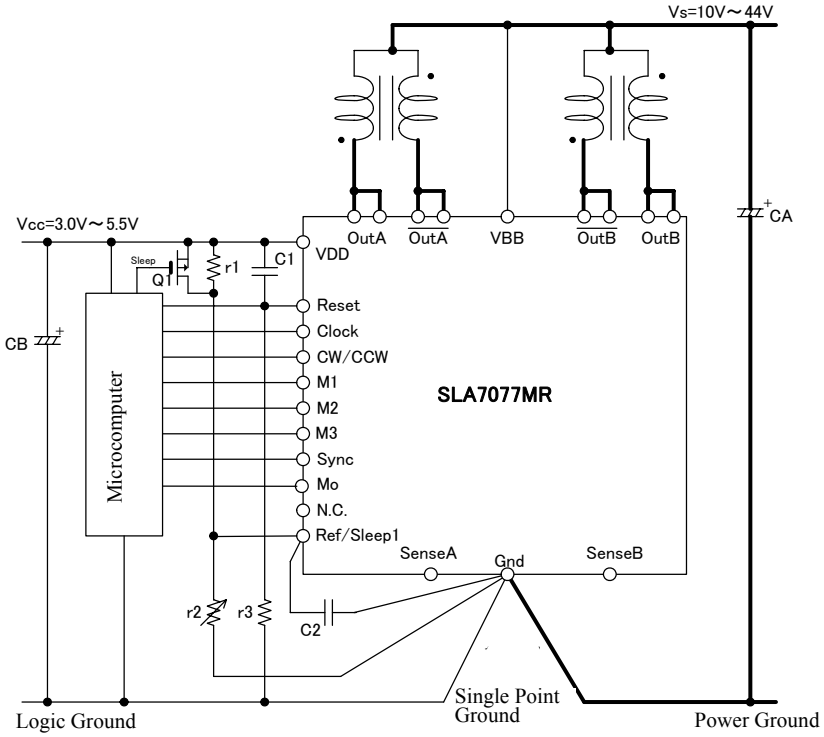


Pin Assignment (Terminal Functions)

Pin No.	Symbol	Function
1, 2	Out A	Phase A Output
3, 4	Out A/	Phase A/ Output
5	Sense A	Phase A Current Sense
6	Mo	Position Monitoring Output
7	M1	Micro-Stepping Operation Mode and Sleep Mode 2 Setting Input
8	M2	
9	M3	
10	Clock	Step Clock Input
11	V_{BB}	Main Power Supply (For Motor)
12	Gnd	GND
13	Ref	Control Current and Sleep Mode 1 Setting Input.
14	V_{DD}	Logic Supply
15	Reset	Reset Input for Logic Circuit
16	CW/CCW	Forward / Reverse Switch Input
17	Sync	PWM Chopping Function Select Input
18	N.C.	Non Connection
19	Sense B	Phase B Current Sense
20, 21	Out B/	Phase B/ Output
22, 23	Out B	Phase B Output

SLA707xM Series

Example application circuit



Reference constant

R_1 = 10kΩ
R_2 = 5.1kΩ(VR)
R_3 = 10kΩ

C_A = 100μF/50V
C_B = 10μF/10V
C_1 = 0.1μF

- Take precautions to avoid noise on the V_{DD} line:
  Switching noise from PCB traces, where high current flows, to the V_{DD} line should be minimized because the noise level more than 0.5V on the V_{DD} line may cause malfunctioning operation.
  The tip for avoiding such problem is to separate the logic GND (S-GND) and the power GND (P-GND) on the PCB, and then connect them together at IC GND pin (pin 12).

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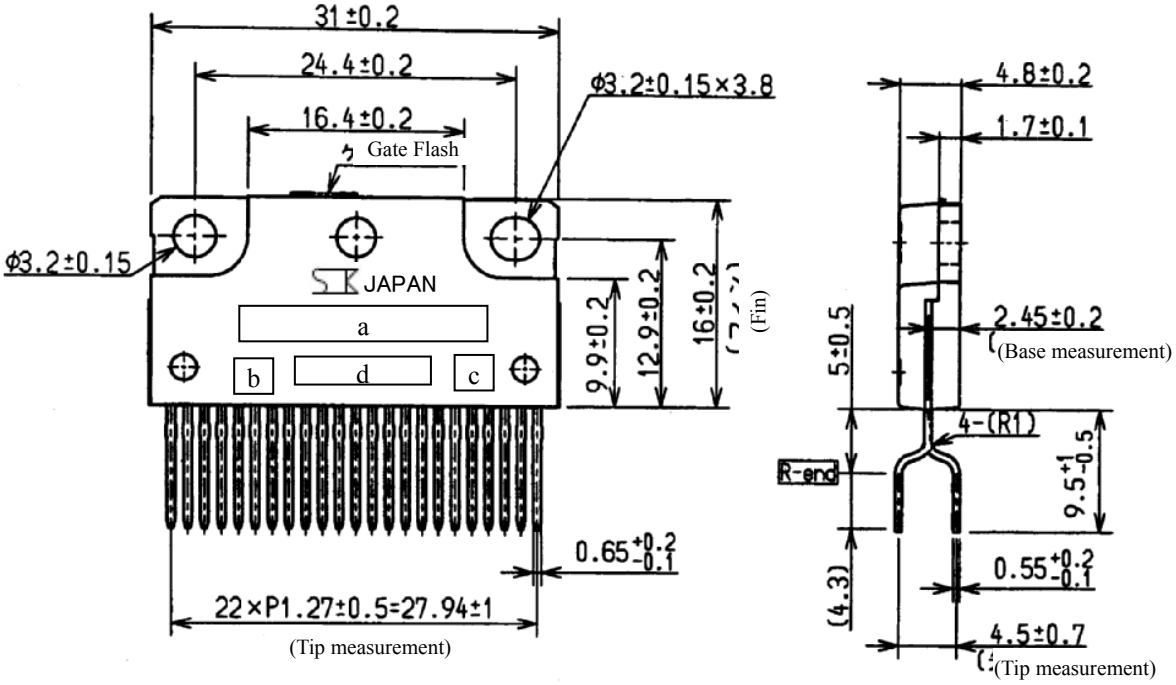
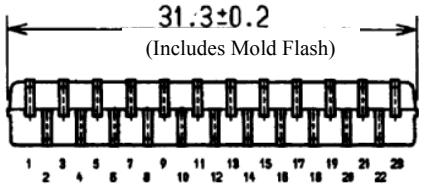
Package information

Package type, physical dimensions and Material





Dimensions in millimeters
Material of terminal : Cu
Treatment of terminal : Ni planting + solder dip (Pb Free)

Appearance

The body shall be clean and shall not bear any stain, rust or flaw.

Marking

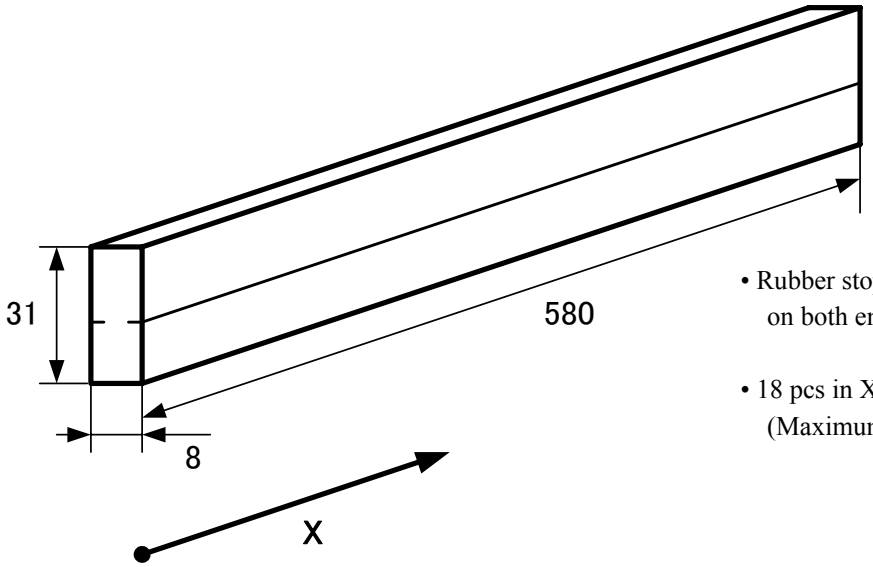
The part number and lot number shall be clearly marked in white.

a. Part Number (1)	SLA707xMR*
b. Part Number (2)	W B (Marked per functions.)*
c. Part Number (3)	P (Marked per functions.)*
d. Lot Number	
1st letter	The last digit of year
2nd letter	Month
	1 to 9 : Arabic Numerals for Jan. to Sep.
	October : O
	November : N
	December : D
3rd &4th letter	Day
	01 to 31 : Arabic Numerals

* The letter x in Part Number (1) represents one number from 0 to 3 and 5 to 8 according to the combination of the current rating and sequencer.
The letter P, R, W, B represent the functions built-in. (No marking for non built-in functions.)

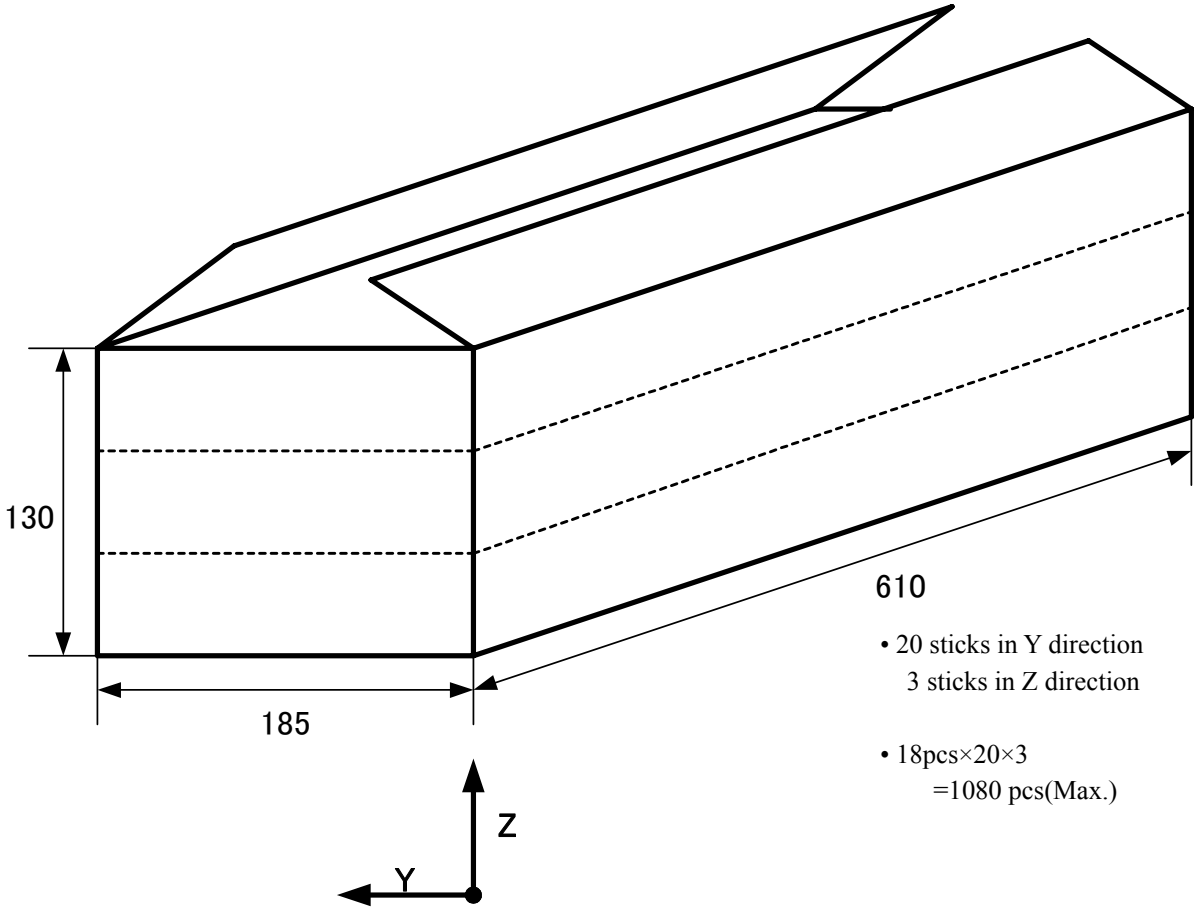
Packing specifications

1



• Rubber stoppers are provided on both ends of a stick.

• 18 pcs in X direction
(Maximum: 18 pcs per stick)



• 20 sticks in Y direction
3 sticks in Z direction

• 18pcs×20×3
=1080 pcs(Max.)

Dimensions in millimeters

Cautions and warnings

The calculation of control current

SLA707xMR control current Io (at Mode F) is calculated as follows:

$$I_O = V_{REF} / R_S$$

Setting the REF voltage more than 2V activates the sleep mode 1 (all outputs are in OFF state).
Even in this case, the internal logic circuit is alive.

Logic input/output (RESET, CLOCK, CW/CCW, M1, M2, M3, SYNC, Mo)

• The timing shown below shall comply with the "Logic input timing".
-The rising edge timing of CW/CCW, M1, M2, M3 and CLOCK input
-The RESET release timing (=the falling edge on RESET input) and the rising edge timing of CLOCK input
*In case the above does not comply with the "Logic input timing", the device may operate with an unexpected sequence.

• Be sure not to leave the logic inputs (RESET, CLOCK, CW/CCW, M1, M2, M3, SYNC) open.
Be sure to connect the unused logic inputs to VDD or GND.
*In case any of the logic inputs are left "OPEN", malfunction may occur due to external noises.

• When the logic output (Mo) is not used, be sure to keep it "OPEN".
*In case it is connected to VDD or GND, it may cause the device's deterioration or/and breakdown.

Mounting on a heat sink

1) Recommended Mounting Torque (on an External Heat sink) 0.490 to 0.822N•m

2) Recommended Silicone

G746	{SHIN-ETSU CHEMICAL}
YG6260	{TOSHIBA SILICONE}
SC102	{DOW CORNING TORAY SILICONE}

Notice

This device has C-MOS inputs. Please note the following contents.

- When a static electricity is liable to be troublesome, especially in winter, be sure to control the room humidity properly.

- Be sure to take some proper measures for wirings from the IC input pins and for assembly processes in order not to apply static charges to IC leads. PC board pins should be shorted together to keep them in the same potential to avoid this kind of trouble.

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